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1 Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Complete if Known <table border="1"> <tr> <td>Application Number</td> <td>10/766,765</td> </tr> <tr> <td>Filing Date</td> <td>28 January 2004</td> </tr> <tr> <td>First Named Inventor</td> <td>Frederick A. Ware</td> </tr> <tr> <td>Group Art Unit</td> <td>2631</td> </tr> <tr> <td>Examiner Name</td> <td>GHAYOUR, MOHAMMAD H</td> </tr> <tr> <td>Attorney Docket Number</td> <td>RBUS 1310-1</td> </tr> </table>		Application Number	10/766,765	Filing Date	28 January 2004	First Named Inventor	Frederick A. Ware	Group Art Unit	2631	Examiner Name	GHAYOUR, MOHAMMAD H	Attorney Docket Number	RBUS 1310-1
Application Number	10/766,765														
Filing Date	28 January 2004														
First Named Inventor	Frederick A. Ware														
Group Art Unit	2631														
Examiner Name	GHAYOUR, MOHAMMAD H														
Attorney Docket Number	RBUS 1310-1														
Sheet	1	of	2												

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
ULP	A50	5,548,146		Kuroda et al.	08-20-1996	
ULP	A51	6,377,640		Trans	04-23-2002	
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	A18					
	A19					
	A20					

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		Office ³	Number ⁴				
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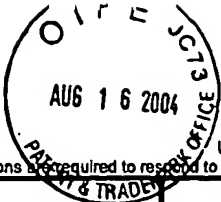
Examiner Signature	ICHAH TRAN	Date Considered	10/12/05
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			Attorney Docket Number	RBUS 1310-1
Sheet	2	of	2	

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
dlf	C27	WIDMER, A.X., et al., "A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code," IBM J. Res. Develop., Vol. 27, No. 5, September 1983, 440-451.	
dlf	C28	BANU, MIHAI, et al., "TA 6.4: A 660Mv/s CMOS Clock Recovery Circuit with Instantaneous Locking for NRZ Data and Burst-Mode Transmission," IEEE International Solid State Circuits Conference, 1993, 102-103, 270.	
dlf	C29	ELDERING, CHARLES A., et al., "Digital Burst Mode Clock Recovery Technique for Fiber-Optic Systems," Journal of Lightwave Technology, Vol. 12, No. 2, February 1994, 271-279.	
dlf	C30	CHANG, KEN K. Y., et al., "A 2 Gb/s Asymmetric Serial Link for High-Bandwidth Packet Switches," Hot Interconnects V, Stanford University, August 1997, 1-9.	
dlf	C31	HU, TIMOTHY H., et al., "A Monolithic 480 Mb/s Parallel AGC/Decision/Clock-Recovery Circuit in 1.2-μ CMOS," IEEE Journal of Solid-State Circuits, Vol. 28, No. 12, December 1993, 1314-1320.	
dlf	C32	KIM, SUNGJOON, et al., "An 800Mbps Multi-Channel CMOS Serial Link with 3x Oversampling," IEEE 1995 Custom Integrated Circuits Conference, 22.7.1-22.7.4.	
dlf	C33	NAKAMURA, KAZUYUKI, et al., "A 6 Gbps CMOS Phase Detecting DEMUX Module Using Half-Frequency Clock," 1998 Symposium on VLSI Circuits Digest of Technical Papers, 196-197.	
dlf	C34	POULTON, JOHN, et al., "A Tracking Clock Recovery Receiver for 4Gb/s Signaling, Hot Interconnects '97, August 21-23, 1997, Palo Alto, CA, 1-13.	
dlf	C35	DALLY, W, et al., "DIGITAL SYSTEMS ENGINEERING," Cambridge University Press, 1998, pages 447-449.	
dlf	C36	CERISOLA, M., et al., "CORD - a WDM Optical Network: Control Mechanism Using Subcarrier Multiplexing and Novel Synchronization Solutions," Communications, 1995. ICC 95 Seattle, Gateway to Globalization, 1995 IEEE International Conference on , Volume: 1 , 18-22 June 1995 Pages:261 - 265 vol.1	

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Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Sheet

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of

Complete if Known

Application Number	10/766,765
Filing Date	28 January 2004
First Named Inventor	Frederick A. Ware
Group Art Unit	2631
Examiner Name	Unassigned
Attorney Docket Number	RBUS 1310-1

U.S. PATENT DOCUMENTS

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		Number	Kind Code ² (if known)			
lll	A1	3,155,102		Niederer, Jr. et al.	11-03-1964	
	A2	3,638,121		Spilker, Jr.	01-25-1972	
	A3	3,922,491		Bjork et al.	11-25-1975	
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lll	A18	2001/0048382		Low et al.	12-06-2001	
lll	A19	2001/0053175		Hector et al.	12-20-2001	
lll	A20	2003/0026399		Carlson	02-06-2003	

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		Office ³	Number ⁴	Kind Code ² (if known)				
lll	B1	JP	02000035831A		Nitsusan Jidosha KK	08-14-1990	Abstract only	
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Signature

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Date
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			Application Number	10766,765
			Filing Date	28 January 2004
			First Named Inventor	Frederick A. Ware
			Group Art Unit	2631
			Examiner Name	Unassigned
Sheet	2	of	Attorney Docket Number	RBUS 1310-1

U.S. PATENT DOCUMENTS						
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		Number	Kind Code ² (if known)			
110	A21	2003/0063597		Suzuki	04-03-2003	
111	A22	2003/0146800		Dvorak	08-07-2003	
112	A23	2003/0198212		Hector et al.	10-23-2003	
113	A24	2003/0198308		Hector et al.	10-23-2003	
114	A25	2004/0032354		Knobel et al.	02-19-2004	
115	A26	2004/0057500		Balachandran et al.	03-25-2004	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Application Number	10/766,765
			Filing Date	28 January 2004
			First Named Inventor	Frederick A. Ware
			Group Art Unit	2631
			Examiner Name	Unassigned
			Attorney Docket Number	RBUS 1310-1
Sheet	3	of		

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
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elt	C1	U.S. Patent Application No. 10/278,708 filed 22 October 2002, entitled "Phase Adjustment Apparatus and Method for a Memory Device Signaling System."	
elt	C2	DANIELE, N. et al., "Principle and Motivations of UWB Technology for High Data Rate WPAN Applications," SOC 2003, 4 pages.	
elt	C3	WIN, MOE Z., et al., "Impulse Radio: How it Works," IEEE Communications Letters 2(2), Feb. 1998, 36-38.	
elt	C4	DANIELE, NORBERT, "Ultra Wide Band Principles and Applications for Wireless Communications," CEA-LETI Annual Review, 25 and 26 June 2002, 24 pages.	
elt	C5	U.S. Patent Application No. 09/941,079 filed 28 August 2001 entitled "Clock Data Recovery with Selectable Phase Control Input."	
elt	C6	Yang, Chih-Kong Ken "Design of High-Speed Serial Links in CMOS" Technical Report No. CSL-TR-98-775, Sponsored By Center for Integrated Systems, Sun Microsystems and LSI Logic Inc. December 1998, pp. 1-182.	
elt	C7	RaSer™ X Product Brief, "Highly Flexible 10 Gbps Backplane Serial Link Interface," Copyright 2003 Rambus, Inc., all rights reserved, 2 pages.	
elt	C8	Yellowstone Technology Brief, "High Performance Memory Interface Technology," Copyright 2003 Rambus, Inc., all rights reserved, 2 pages.	
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	C10		
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		RBUS 1310-1				
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First Named Inventor		Frederick A. Ware				
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UK	A1	4,384,354		Crawford et al.	05/17/1983	
	A2	5,122,978		Merrill	06/16/1992	
	A3	5,436,908		Fluker et al.	07/25/1995	
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	A9	6,396,329		Zerbe	05/28/2002	
	A10	6,442,644		Gustavson et al.	08/27/2002	
	A11	6,448,815		Talbot et al.	09/10/2002	
	A12	6,463,392		Nygaard et al.	10/08/2002	
	A13	6,469,555		Lau et al.	10/22/2002	
	A14	6,473,439		Zerbe et al.	10/29/2002	
	A15	6,510,503		Gillingham et al.	01/21/2003	
	A16	6,539,072		Donnelly et al.	03/25/2003	
	A17	6,556,934		Higashide	04/29/2003	
	A18	6,643,787		Zerbe et al.	11/04/2003	
	A19	2003/0026399		Carlson	02/06/2003	

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llt	C1	PARIS, LLUIS ET AL, "WP 24.3 A 800MB/s 72Mb SLD RAM with Digitally-Calibrated DLL," IEEE International Solid-State Circuits Conference (1999), 13 pages.	
llt	C2	NAKASE, YASUNOBU ET AL, "Source-Synchronization and Timing Vernier Techniques for 1.2-GB/s SLD RAM Interface," IEEE Journal of Solid-State Circuits, Vol. 34, No. 4 (Apr. 1999), 494-501.	
llt	C3	GILLINGHAM, PETER, "SLDRAM Architectural and Functional Overview," SLD RAM Consortium (29 Aug 1997), 1-14.	
llt	C4	"Draft Standard for a High-Speed Memory Interface (SyncLink)", Draft 0.99 IEEE P1596.7-199X (1996), 56 pages	
llt	C5	GILLINGHAM, PETER, "SLDRAM: High-Performance, Open-Standard Memory," IEEE (1997), 29-39	
llt	C6	SLDRAM Inc., "400 Mb/s/pin SLD RAM," Draft Advance (9 Jul 1998), 1-69.	
llt	C7	ZERBE, JARED ET AL., U.S. Patent Application No. 09/776,550 filed 2 February 2001, entitled "Method and Apparatus for Evaluating and Calibrating a Signaling System."	
llt	C8	ZERBE, JARED ET AL, U.S. Patent Application No. 09/976,170 filed 21 October 2001, entitled "Method and Apparatus for Evaluating and Optimizing a Signaling System."	
llt	C9	RAMBUS "Direct Rambus Short Channel Layout Guide, Version 0.95" (August 2001), 40 pages	
llt	C10	RAMBUS "Direct Rambus Long Channel Design Guide" (2000), 45 pages	
llt	C11	RAMBUS, INC. "RDRAM Direct Rambus Clock Generator" (April 2002), 22 pages	

Examiner Signature	KHAN TRAN	Date Considered	10/12/05
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		Application Number	
		Filing Date	28 January 2004 (Herewith)
		First Named Inventor	Frederick A. Ware
		Group Art Unit	
		Examiner Name	
		Attorney Docket Number	RBUS 1310-1
Sheet	4	of	4

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Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
llt	C12	RDRAM® Overview, "High Performance Memory Interface Solution", Copyright 2003 Rambus, Inc., all rights reserved, 4 pages	
llt	C13	REDWOOD TECHNOLOGY BRIEF "High Performance Parallel Bus Interface Technology", Copyright 2003 Rambus, Inc., all rights reserved, 2 pages.	
llt	C14	LEWIS, DAVE, "Easy-to-Use LVDS Serdes for the Serdes Neophyte" National Semiconductor, (16 June 2003), pp. 1-5.	
llt	C15	INTEL "How to Measure RDRAM* System Clock Jitter" Application Note AP-667 (June 1999), pp. 1-15	

Examiner Signature	KHAH TRAN	Date Considered	10/12/05
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Sheet	1	of	2
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Application Number	10/766,765
Filing Date	28 January 2004
First Named Inventor	Frederick A. Ware
Art Unit	Unassigned
Examiner Name	Unassigned
Attorney Docket Number	RBUS 1310-1

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KHAI TRAN

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		Application Number	10/766,765
		Filing Date	28 January 2004
		First Named Inventor	Frederick A. Ware
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		Examiner Name	Unassigned
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KHA	C1	U.S. Patent Application No. 10/278,478, Filed 22 October 2002 entitled "Timing Calibration Apparatus and Method for a Memory Device Signaling System"	
WU	C2	Chang, Kun-Yung "Design of a CMOS Asymmetric Serial Link" A Dissertation Submitted to the Department of Electrical Engineering and the Committee on Graduate Studies of Stanford University August 1999, 119 pages	

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